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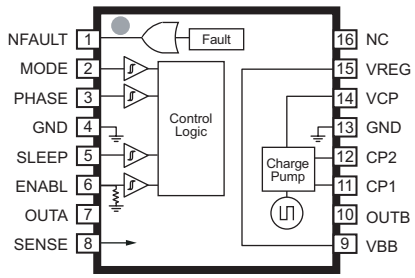
Preliminary Data Sheet
Subject to Change without Notice
November 4, 2005

A3950

DMOS Full-Bridge Motor Driver

Package LP, 16-pin TSSOP
with Exposed Thermal Pad



Approximate Scale 1:1

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB}	**36 V**
Output Current, I_{OUT}	**2.8 A**
Sense Voltage, V_{SENSE}	**±500 mV**
VBB to OUT*x*	**36 V**
OUT*x* to SENSE	**36 V**
Logic Input Voltage, V_{IN}	**–0.3 to 7 V**
Operating Temperature Range	
Ambient, T_A, Range S	**–20°C to 85°C**
Junction Temperature, $T_{J(MAX)}$	**150°C**
Storage Temperature, T_S	**–40°C to 125°C**

Designed for PWM (pulse width modulated) control of dc motors, the A3950 is capable of peak output currents to ±2.8 A and operating voltages to 36 V.

PHASE and ENABLE input terminals are provided for use in controlling the speed and direction of a dc motor with externally applied PWM control signals. Internal synchronous rectification control circuitry is provided to lower power dissipation during PWM operation.

Internal circuit protection includes motor lead short-to-supply / short-to-ground, thermal shutdown with hysteresis, undervoltage monitoring of V_{BB} and V_{CP}, and crossover-current protection.

The A3950 is supplied in a thin profile (<1.2 mm overall height) 16-pin TSSOP package with exposed thermal pad (package LP). It is lead (Pb) free with 100% matte tin leadframe plating.

FEATURES

- Low $R_{DS(on)}$ outputs
- Overcurrent protection
- Motor lead short-to-supply protection
- Short-to-ground protection
- Sleep function
- Synchronous rectification
- Diagnostic output
- Internal UVLO
- Crossover-current protection

Use the following complete part numbers when ordering:

Part Number	Packing
A3950SLP-T	96 pieces / tube
A3950SLPTR-T	13-in. reel, 4000 pieces / reel

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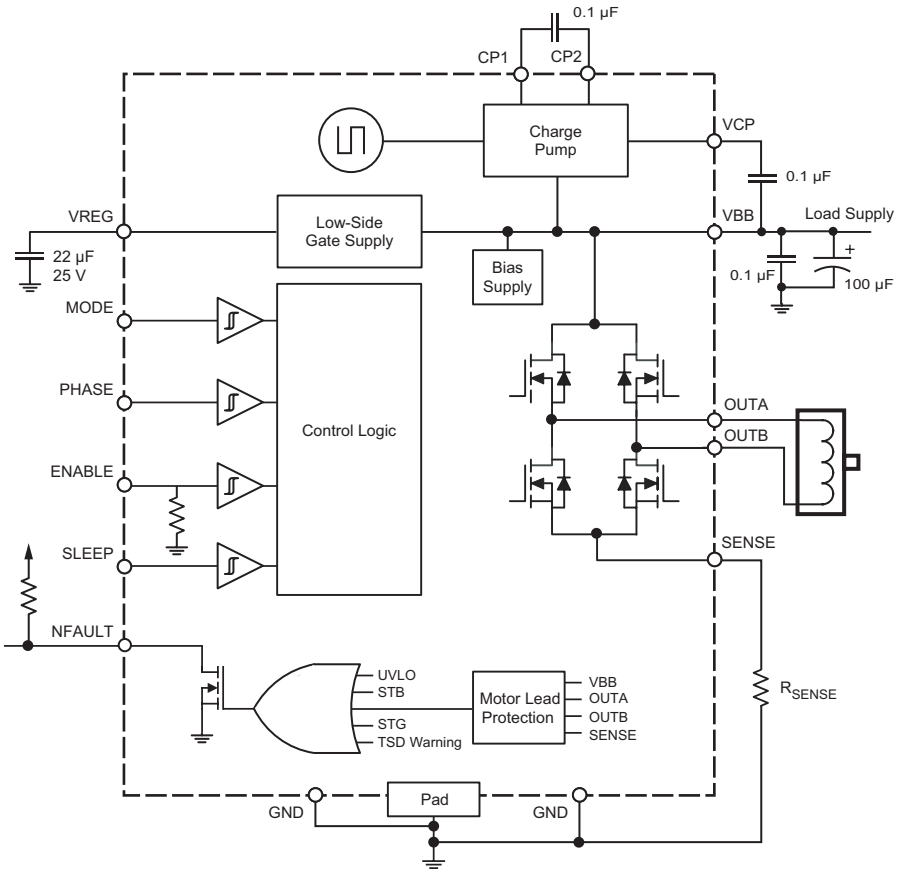
Functional Block Diagram



Control Logic Table[1]

Pin						Function
PHASE	ENABLE	MODE	SLEEP	OUTA	OUTB	
1	1	X	1	H	L	Forward
0	1	X	1	L	H	Reverse
X	0	1	1	L	L	Brake (slow decay)
1	0	0	1	L	H	Fast Decay Synchronous Rectification[2]
0	0	0	1	H	L	Fast Decay Synchronous Rectification[2]
X	X	X	0	Z	Z	Sleep Mode

1X iindicates "don't care," Z indicates high impedence.
2To prevent reversal of current during fast decay synchronous rectification, outputs go to the high impedance state as the current approaches 0 A.

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ELECTRICAL CHARACTERISTICS at T_J = 25°C, V_{BB} = 8 to 36 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	6	8.5	mA
		Charge pump on, outputs disabled	–	3	4.5	mA
		Sleep mode	–	–	10	µA
PHASE, ENABLE, MODE Input Voltage	V_{IH}		2.0	–	–	V
	V_{IL}		–	–	0.8	V
SLEEP Input Voltage	V_{IH}		2.7	–	–	V
	V_{IL}		–	–	0.8	V
PHASE, MODE Input Current[1]	I_{IH}	V_{IN} = 2.0 V	–	<1.0	20	µA
	I_{IL}	V_{IN} = 0.8 V	–	<–2.0	–20	µA
ENABLE Input Current	I_{IH}	V_{IN} = 2.0 V	–	40	100	µA
	I_{IL}	V_{IN} = 0.8 V	–	16	40	µA
SLEEP Input Current	I_{IH}	V_{IN} = 2.7 V	–	27	50	µA
	I_{IL}	V_{IN} = 0.8 V	–	<1	10	µA
NFAULT Output Voltage	V_{OL}	I_{sink} = 1.0 mA	–	–	0.4	V
Input Hysteresis, except SLEEP	V_{IHys}		100	150	200	mV
Output On Resistance	$R_{DS(on)}$	Source driver, I_{OUT} = -2.8 A, T_J=25°C	–	0.35	0.48	Ω
		Source driver, I_{OUT} = -2.8 A, T_J=125°C	–	0.55	0.8	Ω
		Sink driver, I_{OUT} = 2.8 A, T_J=25°C	–	0.3	0.43	Ω
		Sink driver, I_{OUT} = 2.8 A, T_J=125°C	–	0.45	0.7	Ω
Propagation Delay Time	t_{pd}	PWM, change to source or sink ON	–	600	–	ns
		PWM, change to source or sink OFF	–	100	–	ns
Crossover Delay	t_{COD}		–	500	–	ns
Protection Circuitry						
UVLO Threshold	V_{UV}	V_{BB} increasing	–	6.5	–	V
UVLO Hysteresis	V_{UVHys}		–	250	–	mV
Overcurrent Threshold[2]	I_{OCP}		3	–	–	A
Overcurrent Protection Period	t_{OCP}		–	1.2	–	ms
Thermal Warning Temperature	T_{JW}	Temperature increasing	–	160	–	°C
Thermal Warning Hysteresis	T_{JWHys}	Recovery = T_{JW} – T_{JWHys}	–	15	–	°C
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	175	–	°C
Thermal Shutdown Hysteresis	$T_{JTSDHys}$	Recovery = T_{JTSD} – $T_{JTSDHys}$	–	15	–	°C

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2]Overcurrent protection is tested at 25°C in a restricted range and guaranteed by characterization.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	34	ºC/W
		2-layer PCB with 3.8 in.^{2} copper both sides, connected by thermal vias	43	ºC/W

*Additional thermal data available on the Allegro Web site.

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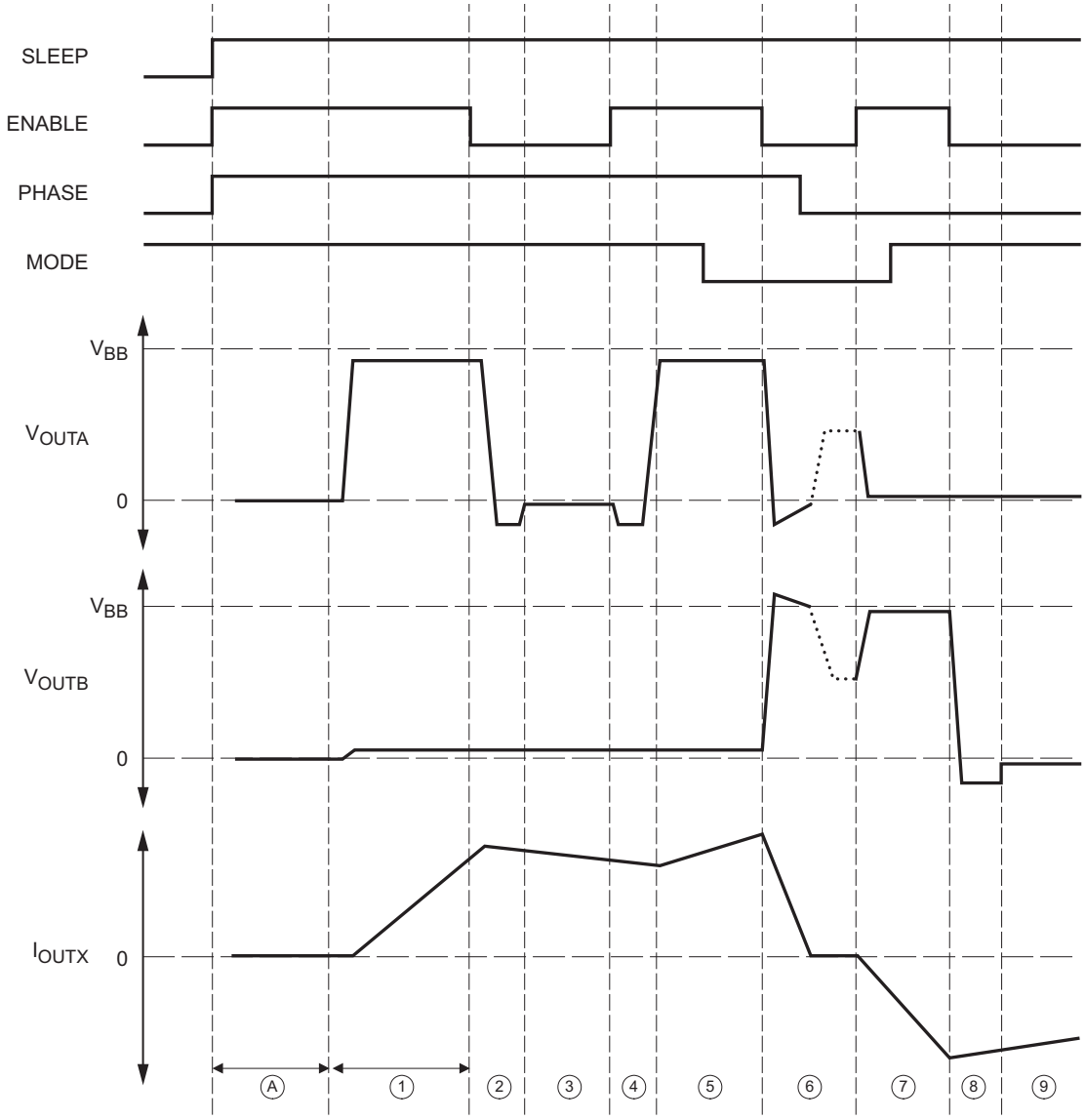
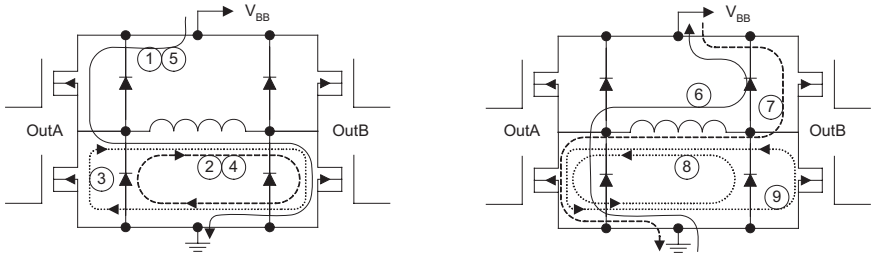
Timing Diagram: PWM Control





Ⓐ Charge pump and VREG power-on delay (≈200 µs)

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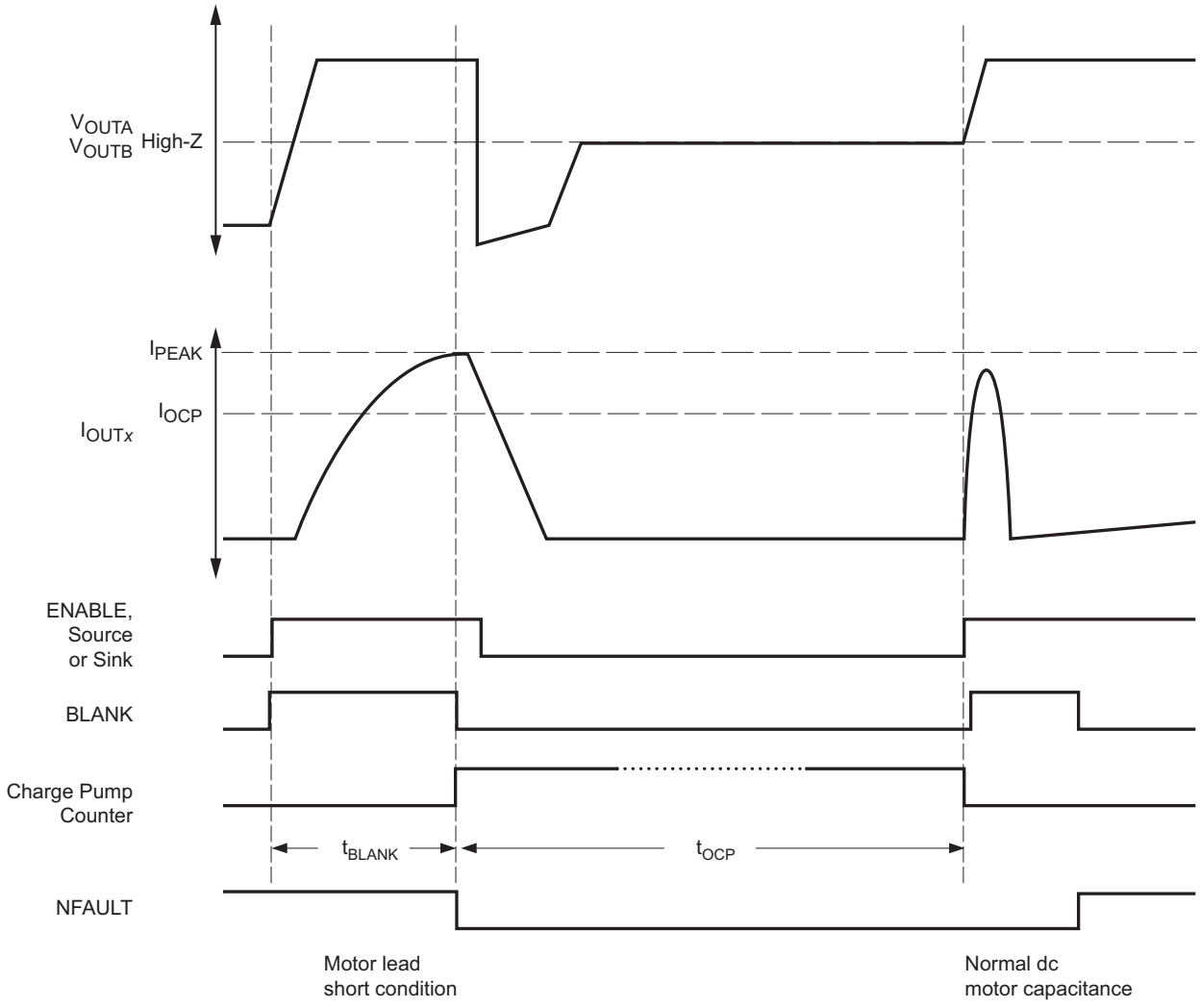
Timing Diagram: Overcurrent Control



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Functional Description

VREG. This supply voltage is used to run the sink-side DMOS outputs. VREG is internally monitored and in the case of a fault condition, the outputs of the device are disabled. The VREG pin should be decoupled with a 0.22 µF capacitor to ground.

Charge Pump. The charge pump is used to generate a supply above V_{BB} to drive the source-side DMOS gates. A 0.1 µF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1 µF ceramic monolithic capacitor should be connected between VCP and VBB to act as a reservoir to run the high-side DMOS devices. The VCP voltage level is internally monitored and, in the case of a fault condition, the outputs of the device are disabled.

Shutdown. In the event of a fault due to excessive junction temperature, or low voltage on VCP or VREG, the outputs of the device are disabled until the fault condition is removed. At power-on the UVLO circuit disables the drivers.

Sleep Mode. Control input SLEEP is used to minimize power consumption when the A3950 not in use. This disables much of the internal circuitry, including the regulator and charge pump. A logic low setting puts the device into Sleep mode, and a logic high setting allows normal operation. After coming out of Sleep mode, provide a 1 ms interval before applying PWM signals, to to allow the charge pump to stabilize.

MODE. Control input MODE is used to toggle between fast decay mode and slow decay mode. A logic high puts the device in slow decay mode. Synchronus rectification is always enabled.

Braking. The braking function is implemented by driving the device in slow decay mode via the MODE setting and applying an enable chop command. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts out the motor generated BEMF as long as the ENABLE chop mode is asserted. The maximum current can be approximated by V_{BEMF}/R_L. Care should be taken to insure that the maximum ratings of the device are not exceeded in worse case braking situations: high speed and high-inertia loads.

Overcurrent Protection. The voltage on the output pins relative to supply are monitored to ensure that the motor lead is not shorted to supply or ground. If a short is detected, the full-bridge outputs are turned off, flag NFAULT is driven low, and a 1.2 ms fault timer is started.

After this 1.2 ms period, t_{OCP}, the device will then be allowed to follow the input commands and another turn-on is attempted. If there is still a fault condition, the cycle repeats. If, after t_{OCP} expires, it is determined that the short condition is not present, the NFAULT pin is released and normal operation resumes.

Diagnostic Output. The NFAULT pin signals a problem with the chip via an open drain output. A motor fault, undervoltage condition, or $T_J > 160°C$ will drive the pin active low. This output is not valid when SLEEP puts the device into minimum power dissipation mode.

TSD. Two die temperature monitors are integrated on the chip. As die temperature increases towards the maximum, a thermal warning signal will be triggered at 160°C. This fault drives the NFAULT low, but does not disable the operation of the chip. If the die temperature increases further, to approximately 175°C, the full-bridge outputs will be disabled until the internal temperature falls below a hysteresis of 15°C.

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Applications Information

Power Dissipation. First order approximation of power dissipation in the A3950 can be calculated by first examining the power dissipation in the full-bridge during each of the operation modes. The A3950 features synchronous rectification, a feature that effectively shorts out the body diode by turning on the low $R_{DS(on)}$ DMOS driver during the decay cycle. This significantly reduces power dissipation in the full-bridge. In order to prevent shoot-through, where both source and sink driver are on at the same time, the A3950 implements a 500 ns typical crossover delay time. For this period, the body diode in the decay current path conducts the current until the DMOS driver turns on. This does affect power dissipation and may need to be considered in high current, high ambient temperature applications. In addition, motor parameters and switching losses can add power dissipation that could affect critical applications.

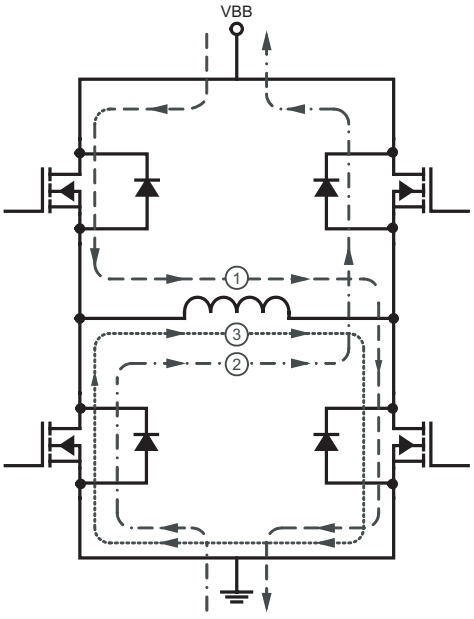

Figure 1. Current Decay Patterns

Drive Current. This current path is through source DMOS driver, motor winding, and sink DMOS driver. Power dissipation is I^2R loses in one source and one sink DMOS driver, as shown in the following equation:

$$P_D = I^2(R_{DS(on)Source} + R_{DS(on)Sink}) \quad (1)$$

Fast Decay with Synchronous Rectification. This decay mode is equivalent to a phase change where the opposite drivers are switched on. When in fast decay, the motor current is not allowed to go negative (direction change). Instead, as the current approaches zero, the drivers turn off. The power calculation is the same as the drive current calculation, equation 1:

Slow Decay SR (Brake Mode). In this decay mode, both sink drivers turn on, allowing the current to circulate through the sink drivers and the load. Power dissipation is I^2R loses in the two sink DMOS drivers:

$$P_D = I^2(2 \times R_{DS(on)Sink}) \quad (2)$$

Layout. The printed circuit board should include a heavy ground plane. For optimum electrical and thermal performance, the exposed thermal pad of the device should be soldered directly to an exposed copper area directly under the device. The load supply pin, VBB, should be decoupled with an electrolytic capacitor (typically 100 µF) in parallel with a ceramic capacitor placed as close as possible to the device. The ceramic capacitors between VCP and VBB, connected to VREG, and between CP1 and CP2, should be as close to the pins of the device as possible, in order to minimize lead inductance.

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Ground. A star ground should be located as close to the A3950 as possible. The copper ground plane directly under the exposed thermal pad makes a good location for the star ground point. The exposed pad can be connected to ground for this purpose.

SENSE Pin. A low value resistor can be placed between the SENSE pin and ground for current sensing purposes. To minimize ground-trace IR drops in sensing the output current level, the current sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low value sense resistors, the IR drops in the PCB can be significant, and should be taken into account.

When selecting a value for the sense resistor be sure not to exceed the maximum voltage on the SENSE pin of ±500 mV.

Terminal List Table

Name	Number	Description
NFAULT	1	Fault output, open drain
MODE	2	Logic input
PHASE	3	Logic input for direction control
GND	4	Ground
SLEEP	5	Logic input
ENABLE	6	Logic input
OUTA	7	DMOS full-bridge output A
SENSE	8	Power return
VBB	9	Load supply voltage
OUTB	10	DMOS full-bridge output B
CP1	11	Charge pump capacitor terminal
CP2	12	Charge pump capacitor terminal
GND	13	Ground
VCP	14	Reservoir capacitor terminal
VREG	15	Regulator decoupling terminal
NC	16	No connection
Pad	–	Exposed pad for thermal dissipation connect to pins 4,13

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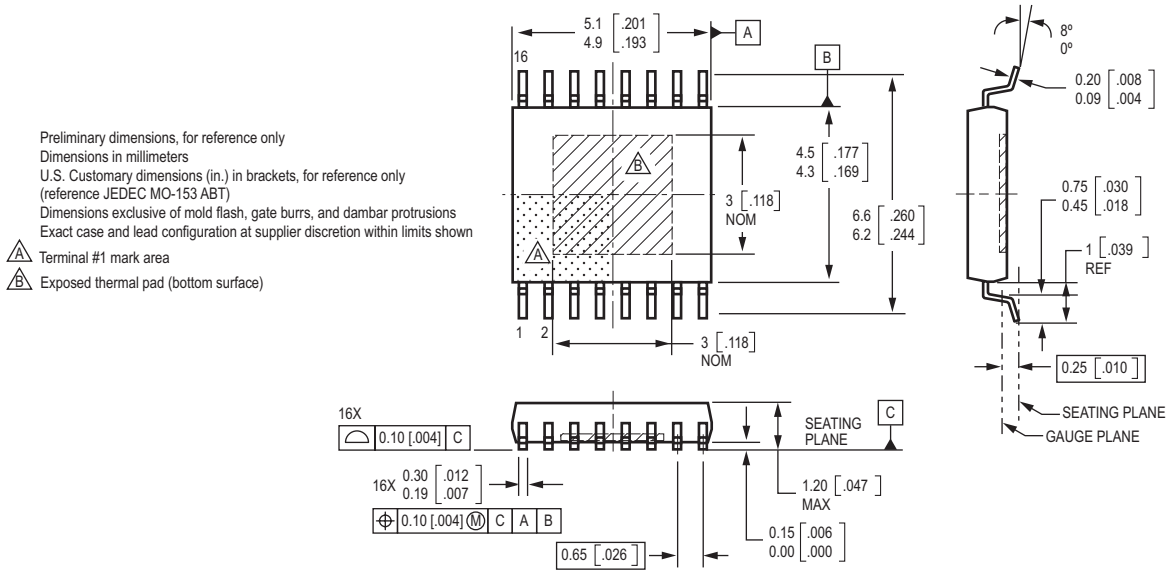
DMOS Full-Bridge Motor Driver

LP Package, 16-Pin TSSOP with Exposed Thermal Pad


Preliminary dimensions, for reference only
Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only
(reference JEDEC MO-153 ABT)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area
B Exposed thermal pad (bottom surface)
5.1 4.9 .201 .193
16
1 2
3 .118 NOM
4.5 4.3 .177 .169
6.6 6.2 .260 .244
8° 0°
0.20 0.09 .008 .004
0.75 0.45 .030 .018
1 .039 REF
0.25 .010
SEATING PLANE
GAUGE PLANE
16X
0.10 [.004] C
16X 0.30 0.19 .012 .007
0.10 [.004] M C A B
0.65 .026
SEATING PLANE
1.20 .047 MAX
0.15 0.00 .006 .000

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